Amendments to the Claims:

In the claims:

Please AMEND Claims 1, 12, and 23 as follows such that the pending claims will read as follows:

Claim 1 (Currently Amended): A method of self-adjusting allocation of memory bandwidth in a network processor system comprising:

determining an amount of memory bandwidth of a network processor allocated among a plurality of data types used to transmit data through a plurality of active ports;

determining an amount of memory bandwidth of [[a]] the network processor used by each of the [[a]] plurality of data types; and

dynamically adjusting the amount of memory bandwidth allocated to at least one of the plurality of data types based on the ~~determination~~ determinations.

Claim 2 (Original): The method of claim 1 wherein a total amount of memory bandwidth of the network processor used by the plurality of data types is configurable.

Claim 3 (Original): The method of claim 2 further comprising determining whether memory bandwidth may be allocated to at least one of the plurality of data types.

Claim 4 (Original): The method of claim 3 wherein determining whether memory bandwidth may be allocated to at least one of the plurality of data types includes determining a difference between a maximum amount of memory bandwidth of the network processor that may be used by the plurality of data types and the total

amount of memory bandwidth of the network processor currently used by the plurality of data types.

Claim 5 (Original): The method of claim 3 wherein determining whether memory bandwidth may be allocated to at least one of the plurality of data types includes determining whether a port for transmitting data of at least one of the plurality data types may be activated.

Claim 6 (Original): The method of claim 1 wherein determining an amount of memory bandwidth of a network processor used by each of a plurality of data types includes:

determining a number of active ports of the network processor used to transmit data of each of the plurality of data types; and

determining an amount of memory bandwidth allocated to each active port for each of the plurality of data types.

Claim 7 (Original): The method of claim 6 wherein the amount of memory bandwidth allocated to each active port for a data type is the same.

Claim 8 (Original): The method of claim 6 wherein the amount of memory bandwidth allocated to each active port for an ATM protocol data type is configurable.

Claim 9 (Original): The method of claim 1 wherein the plurality of data types includes at least one of an ATM protocol data type and an Ethernet protocol data type.

Claim 10 (Original): The method of claim 9 wherein the Ethernet protocol data type includes at least one of a Gigabit Ethernet data type and a Fast Ethernet data type.

Claim 11 (Original): The method of claim 1 wherein dynamically adjusting the amount of memory bandwidth allocated to at least one of the plurality of data types based on the determination includes at least one of dynamically activating and deactivating a port for transmitting data of at least one of the plurality of data types.

Claim 12 (Currently Amended): An apparatus comprising:

port activation logic, adapted to couple to a memory of a network processor and to interact with the memory so as to:

determine an amount of memory bandwidth of the network processor allocated among a plurality of data types used to transmit data through a plurality of active ports;

determine an amount of memory bandwidth of the network processor used by each of the [[a]] plurality of data types; and

dynamically adjust the amount of memory bandwidth allocated to at least one of the plurality of data types based on the ~~determination~~ determinations.

Claim 13 (Original): The apparatus of claim 12 wherein a total amount of memory bandwidth of the network processor used by the plurality of data types is configurable.

Claim 14 (Original): The apparatus of claim 13 wherein the port activation logic is further adapted to determine whether memory bandwidth may be allocated to at least one of the plurality of data types.

Claim 15 (Original): The apparatus of claim 14 wherein the port activation logic is further adapted to determine a difference between a maximum amount of memory bandwidth of the network processor that may be used by the plurality of data types and the total amount of memory bandwidth of the network processor currently used by the plurality of data types.

Claim 16 (Original): The apparatus of claim 14 wherein the port activation logic is further adapted to determine whether a port for transmitting data of at least one of the plurality data types may be activated.

Claim 17 (Original): The apparatus of claim 12 wherein the port activation logic is further adapted to:

determine a number of active ports of the network processor used to transmit data of each of the plurality of data types; and

determine an amount of memory bandwidth allocated to each active port for each of the plurality of data types.

Claim 18 (Original): The apparatus of claim 17 wherein the amount of memory bandwidth allocated to each active port for a data type is the same.

Claim 19 (Original): The apparatus of claim 17 wherein the amount of memory bandwidth allocated to each active port for an ATM protocol data type is configurable.

Claim 20 (Original): The apparatus of claim 12 wherein the plurality of data types includes at least one of an ATM protocol data type and an Ethernet protocol data type.

Claim 21 (Original): The apparatus of claim 20 wherein the Ethernet protocol data type includes at least one of a Gigabit Ethernet data type and a Fast Ethernet data type.

Claim 22 (Original): The apparatus of claim 12 wherein the port activation logic is further adapted to at least one of dynamically activate and deactivate a port for transmitting data of at least one of the plurality of data types.

Claim 23 (Currently Amended): A network processor system comprising:

a memory; and

a network processor coupled to the memory, the network processor comprising:

a memory controller;

a plurality of ports; and

port activation logic, coupled to the memory controller, the plurality of ports and the memory, and adapted to interact with the memory so as to:

determine an amount of memory bandwidth of the network processor allocated among a plurality of data types used to transmit data through a plurality of active ports;

determine an amount of memory bandwidth of the network processor ~~memory~~ used by each of the [[a]] plurality of data types; and

dynamically adjust the amount of memory bandwidth allocated to at least one of the plurality of data types based on the ~~determination~~ determinations.